ABSTRACT OF THE DISCLOSURE

An orthogonal code generating circuit 10 is arranged by a counter circuit unit 12, a combination circuit unit 14 of orthogonal codes, and a control circuit unit 16. Furthermore, the combination circuit unit 14 is constructed of an AND gate 14a and an exclusive-OR gate 14b. The control circuit unit 16 outputs a decode output in response to a set code designation signal CN_0. When a code generation starting signal ST is inputted, a counter circuit 12 starts to output a counter output. Both the decode output and the counter output are entered to the combination circuit unit 14 which AND-gates the corresponding output bits with each other, and thereafter, exclusively OR-gates the AND-gated outputs, and then outputs the exclusively OR-gated signal as serial data of an orthogonal code. As a consequence, since the conventional ROM unit for storing thereinto the orthogonal codes can be omitted, the circuit scale of the orthogonal code generating circuit 10 can be reduced.